Chapter overview

This chapter provides an overview of setting up analyses and starting simulation that applies to any analysis type. The other chapters in Part three, Setting Up and Running Analyses provide specific analysis setup information for each analysis type.

This chapter includes the following sections:

- Analysis types on page 280
- Setting up analyses on page 282
- Starting a simulation on page 290
Analysis types

PSpice A/D supports analyses that can simulate analog-only, mixed-signal, and digital-only circuits.

PSpice A/D fully supports digital analysis by simulating the timing behavior of digital devices within a standard transient analysis, including worst-case (min/max) timing. For mixed analog/digital circuits, all of the above-mentioned analyses can be run. If the circuit is digital-only, only the transient analysis can be run.

Table 22 provides a summary of the available PSpice A/D analyses and the corresponding Analysis type options where the analysis parameters are specified. In Capture, switch to the PSpice view, then from the PSpice menu, choose New Simulation Profile.
The waveform analyzer calculates and displays the results of PSpice A/D simulations for swept analyses. The waveform analyzer also generates supplementary analysis information in the form of lists and tables, and saves this in the simulation output file.

### Table 22  Classes of PSpice A/D analyses

<table>
<thead>
<tr>
<th>Analysis</th>
<th>Analysis type or Option</th>
<th>Swept variable</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Standard analyses</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC sweep</td>
<td>DC Sweep</td>
<td>source parameter temperature</td>
</tr>
<tr>
<td>Bias point</td>
<td>Bias Point</td>
<td></td>
</tr>
<tr>
<td>Small-signal DC transfer</td>
<td>Bias Point</td>
<td></td>
</tr>
<tr>
<td>DC sensitivity</td>
<td>Bias Point</td>
<td></td>
</tr>
<tr>
<td>Frequency response</td>
<td>AC Sweep/Noise</td>
<td>frequency</td>
</tr>
<tr>
<td>Noise (requires a frequency</td>
<td>AC Sweep/Noise</td>
<td>frequency</td>
</tr>
<tr>
<td>response analysis)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient response</td>
<td>Time Domain (Transient)</td>
<td>time</td>
</tr>
<tr>
<td>Fourier (requires transient</td>
<td>Time Domain (Transient)</td>
<td>time</td>
</tr>
<tr>
<td>response analysis)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Simple multi-run analyses</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parametric</td>
<td>Parametric Sweep</td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td>Temperature (Sweep)</td>
<td></td>
</tr>
<tr>
<td><strong>Statistical analyses</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Monte Carlo</td>
<td>Monte Carlo/Worst Case</td>
<td></td>
</tr>
<tr>
<td>Sensitivity/worst-case</td>
<td>Monte Carlo/Worst Case</td>
<td></td>
</tr>
</tbody>
</table>

**Note**  Parametric Analysis is not supported in PSpice A/D Basics.

**Note**  Monte Carlo/Worst Case Analysis is not supported in PSpice A/D Basics.
Chapter 8  Setting up analyses and starting simulation

Setting up analyses

To set up one or more analyses

1. From the PSpice menu, choose New Simulation Profile.
2. Enter the name of the profile and click OK.
3. Click the Analysis tab if it is not already the active tab in the dialog box.
4. Enter the necessary parameter values and select the appropriate check boxes to complete the analysis specifications.
5. Set up any other analyses you want to perform for the circuit by selecting any of the remaining analysis types and options, then complete their setup dialog boxes.

Specific information for setting up each type of analysis is discussed in the following chapters.

See Output variables on page 284 for a description of the output variables that can be entered in the Simulation Settings dialog box displayed for an analysis type.

Specific information for setting up each type of analysis is discussed in the following chapters.
Execution order for standard analyses

For normal simulations that are run from a simulation profile, or in batch mode, only the particular analysis type that is specified will be executed.

During simulation of a circuit file, the analysis types are performed in the order shown in Table 23. Each type of analysis is conducted only once per run.

Several of the analyses (small-signal transfer, DC sensitivity, and frequency response) depend upon the bias point calculation. Because so many analyses use the bias point, PSpice A/D calculates this automatically. PSpice A/D’s bias point calculation computes initial states of digital components as well as the analog components.

Table 23  Execution order for standard analyses

1. DC sweep
2. Bias point
3. Frequency response
4. Noise
5. DC sensitivity
6. Small-signal DC transfer
7. Transient response
8. Fourier components
Output variables

Certain analyses (such as noise, Monte Carlo, sensitivity/worst-case, DC sensitivity, Fourier, and small-signal DC transfer function) require you to specify output variables for voltages and currents at specific points on the schematic. Depending upon the analysis type, you may need to specify the following:

- Voltage on a net, a pin, or at a terminal of a semiconductor device
- Current through a part or into a terminal of a semiconductor device
- A device name

If output variables or other information are required, select Output File Options in the Monte Carlo/Worst Case dialog box and enter the required parameters.

Voltage

Specify voltage in the following format:

\[ v[modifers](<out id>[,<out id>]) \]  

where \(<out id>\) is:

\(<net id>\) or \(<pin id>\)  
\(<net id>\) is a fully qualified net name  
\(<pin id>\) is \(<fully qualified device name>:<pin name>\)

A fully qualified net name (as referred to in line 3 above) is formed by prefixing the visible net name (from a label applied to one of the segments of a wire or bus, or an offpage port connected to the net) with the full hierarchical path, separated by periods. At the top level of hierarchy, this is just the visible name.

A fully qualified device name (from line 4 above) is distinguished by specifying the full hierarchical path followed by the device’s part reference, separated by period characters. For example, a resistor with part reference R34 inside part Y1 placed on a top-level
schematic page is referred to as Y1.R34 when used in an output variable.

A <pin id> (from line 4) is uniquely distinguished by specifying the full part name (as described above) followed by a colon, and the pin name. For example, the pins on a capacitor with reference designator C31 placed on a top-level page and pin names 1 and 2 would be identified as C31:1 and C31:2, respectively.

**Current**

Specify current in the following format:

\[ i[\text{modifiers}](<\text{out device}>[\text{modifiers}]) \]

where \(<\text{out device}\) is a fully qualified device name.

**Modifiers**

The basic syntax for output variables can be modified to indicate terminals of semiconductors and AC specifications. The modifiers come before \(<\text{out id}\) or \(<\text{out device}\). Or, when specifying terminals (such as source or drain), the modifier is the pin name contained in \(<\text{out id}\), or is appended to \(<\text{out device}\) separated by a colon.

Modifiers can be specified as follows:

- For voltage:
  \[ v[\text{AC suffix}](<\text{out id}>[, \text{out id}]) \]
  \[ v[\text{terminal}](<\text{out device}>) \]

- For current:
  \[ i[\text{AC suffix}](<\text{out device}>[:\text{terminal}]) \]
  \[ i[\text{terminal}][\text{AC suffix}](<\text{out device}>) \]

where

\text{terminal} specifies one or two terminals for devices with more than two terminals, such as D (drain), G (gate), S (source)
These building blocks can be used for specifying output variables as shown in Table 24 (which summarizes the accepted output variable formats) and Tables 25 through 28 (which list valid elements for two-terminal, three- or four-terminal devices, transmission line devices, and AC specifications).

**Table 24  PSpice A/D output variable formats**

<table>
<thead>
<tr>
<th>Format</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>V<a href="%20+%20out%20id%20">ac</a></td>
<td>voltage at out id</td>
</tr>
<tr>
<td>V[ac](&lt; +out id &gt;,&lt; - out id &gt;)</td>
<td>voltage across + and - out id’s</td>
</tr>
<tr>
<td>V<a href="%202-terminal%20device%20out%20id%20">ac</a></td>
<td>voltage at a 2-terminal device out id</td>
</tr>
<tr>
<td>V<a href="%203%20or%204-terminal%20device%20out%20id%20">ac</a> or V&lt;x&gt;<a href="%203%20or%204-terminal%20out%20device%20">ac</a></td>
<td>voltage at non-grounded terminal x of a 3 or 4-terminal device</td>
</tr>
<tr>
<td>V&lt;x&gt;&lt;y&gt;<a href="%203%20or%204-terminal%20out%20device%20">ac</a></td>
<td>voltage across terminals x and y of a 3 or 4-terminal device</td>
</tr>
<tr>
<td>V<a href="%20transmission%20line%20out%20id%20">ac</a> or V&lt;z&gt;<a href="%20transmission%20line%20out%20device%20">ac</a></td>
<td>voltage at one end z of a transmission line device</td>
</tr>
<tr>
<td>I[ac](&lt; 3 or 4-terminal out device &gt;:&lt;x&gt;) or I&lt;x&gt;<a href="%203%20or%204-terminal%20out%20device%20">ac</a></td>
<td>current through non-grounded terminal x of a 3 or 4-terminal out device</td>
</tr>
<tr>
<td>I[ac](&lt; transmission line out device &gt;:&lt;z&gt;) or I&lt;z&gt;<a href="%203%20or%204-terminal%20out%20device%20">ac</a></td>
<td>current through one end z of a transmission line out device</td>
</tr>
<tr>
<td>&lt; DC sweep variable &gt;</td>
<td>voltage or current source name</td>
</tr>
<tr>
<td>Device type</td>
<td>&lt;out id&gt; or &lt;out device&gt; device indicator</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td>capacitor</td>
<td>C</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>diode</td>
<td>D</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>voltage-controlled voltage source</td>
<td>E</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>current-controlled current source</td>
<td>F</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>voltage-controlled current source</td>
<td>G</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>current-controlled voltage source</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>independent current source</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>inductor</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>resistor</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>voltage-controlled switch</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>independent voltage source</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>current-controlled switch</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Table 26  Element definitions for 3- or 4-terminal devices**

<table>
<thead>
<tr>
<th>Device type</th>
<th>&lt;out id&gt; or &lt;out device&gt; indicator</th>
<th>&lt;pin id&gt;</th>
<th>Output variable examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs MESFET</td>
<td>B</td>
<td>D (Drain terminal)</td>
<td>V(B11:D)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G (Gate terminal)</td>
<td>ID(B11)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S (Source terminal)</td>
<td></td>
</tr>
<tr>
<td>Junction FET</td>
<td>J</td>
<td>D (Drain terminal)</td>
<td>VG(JFET)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G (Gate terminal)</td>
<td>I(JFET:G)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S (Source terminal)</td>
<td></td>
</tr>
<tr>
<td>MOSFET</td>
<td>M</td>
<td>B (Bulk, substrate terminal)</td>
<td>VDG(M1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>D (Drain terminal)</td>
<td>ID(M1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G (Gate terminal)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S (Source terminal)</td>
<td></td>
</tr>
<tr>
<td>bipolar transistor</td>
<td>Q</td>
<td>B (Base terminal)</td>
<td>V(Q1:B)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C (Collector terminal)</td>
<td>I(Q1:C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>E (Emitter terminal)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S (Source terminal)</td>
<td></td>
</tr>
<tr>
<td>IGBT</td>
<td>Z</td>
<td>C (Collector terminal)</td>
<td>V(Z1:C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>E (Emitter terminal)</td>
<td>I(Z1:C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G (Gate terminal)</td>
<td></td>
</tr>
</tbody>
</table>

**Note**  The IGBT device type is not supported in PSpice A/D Basics.

**Table 27  Element definitions for transmission line devices**

<table>
<thead>
<tr>
<th>Device type</th>
<th>&lt;out id&gt; or &lt;out device&gt; indicator</th>
<th>&lt;z&gt;</th>
<th>Output variable examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>transmission line</td>
<td>T</td>
<td>A (Port A)</td>
<td>V(T32:A+)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B (Port B)</td>
<td>I(T32:B-)</td>
</tr>
</tbody>
</table>
Setting up analyses

The INOISE, ONOISE, DB(INOISE), and DB(ONOISE) output variables are predefined for use with noise (AC sweep) analysis.

<table>
<thead>
<tr>
<th>&lt;ac suffix&gt; device symbol</th>
<th>Meaning</th>
<th>Output variable examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>(none)</td>
<td>magnitude (default)</td>
<td>V(V1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I(V1)</td>
</tr>
<tr>
<td>M</td>
<td>magnitude</td>
<td>VM(CAP1:1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IM(CAP1:1)</td>
</tr>
<tr>
<td>DB</td>
<td>magnitude in decibels</td>
<td>VDB(R1)</td>
</tr>
<tr>
<td>P</td>
<td>phase</td>
<td>IP(R1)</td>
</tr>
<tr>
<td>R</td>
<td>real part</td>
<td>VR(R1)</td>
</tr>
<tr>
<td>I</td>
<td>imaginary part</td>
<td>VI(R1)</td>
</tr>
</tbody>
</table>

Table 28  Element definitions for AC analysis specific elements
Chapter 8 Setting up analyses and starting simulation

Starting a simulation

After you have used Capture to enter your circuit design and have set up the analyses to be performed, you can start a simulation by choosing Run from the PSpice menu. When you enter and set up your circuit this way, Capture automatically generates the simulation files and starts PSpice A/D.

There may be situations, however, when you want to run PSpice A/D outside of Capture. You may want to simulate a circuit that was not created in Capture, for example, or you may want to run simulations of multiple circuits in batch mode.

This section includes the following:

- **Creating a simulation netlist** on page 290
- **Starting a simulation from Capture** on page 299
- **Starting a simulation outside of Capture** on page 299
- **Setting up batch simulations** on page 300
- **The PSpice A/D simulation window** on page 301

Creating a simulation netlist

A netlist is the connectivity description of a circuit, showing all of the components, their interconnections, and their values. When you create a simulation netlist from OrCAD Capture, that netlist describes the current design.

You have a choice between two types of netlist formats:

- a flat netlist
- a hierarchical netlist

The flat netlist is generated for all levels of hierarchy, starting from the top, regardless of whether you are pushed into any level of the hierarchy. Flat netlists are most commonly used as input to PCB layout tools. The flat
simulation netlist format for PSpice contains device entries for all parts on a subcircuit (child) schematic multiple times, once for each instance of the hierarchical part or block used.

The hierarchical netlist preserves the hierarchical information in any subcircuit (child) schematics. It contains a single .SUBCKT definition for each child schematic. The devices in the subcircuit are therefore netlisted only once. Each instance of the hierarchical part or block is then netlisted as an instance of that subcircuit (as an “X” device). The subcircuit name corresponds to the name of the subcircuit (child) schematic. Hierarchical netlists are especially useful to IC designers who want to perform Layout vs. Schematic (LVS) verification because they are more accurate descriptions of the true circuit. The hierarchical netlist format supports LVS tools such as Dracula.

Using netlisting templates

In OrCAD Capture, the PSPICETEMPLATE property specifies how primitive parts are described in the simulation netlist. It defines the pin order and which other part property values to include in the netlist. Only parts with a PSPICETEMPLATE property are included in the simulation. In the process of creating the netlist, buses, connectors, and so on, are resolved.

An alternate template option is provided which allows you to define which netlisting template property to use. This option applies to both flat and hierarchical netlists. With this option, you may specify a particular netlist template for generating netlists that can be used by other simulation tools, for example, or for creating alternate PSpice netlists that contain different part descriptions.

To learn more about using alternate netlist templates, see Specifying alternate netlist templates on page 297.
Passing parameters to subcircuits

Hierarchical netlists have the advantage of allowing parameters to be passed from the top level schematic to any subcircuit schematics. To take advantage of this feature, you must use the new SUBPARAM part in the SPECIAL.OLB library.

Note Hierarchical netlists do not support cross-probing from a subcircuit, nor do they support Probe markers in a subcircuit.

With the SUBPARAM part, you can pass parameters from the top-level schematic to a subcircuit schematic. This allows you to explicitly define the properties and default values to be used during netlisting and simulation.

To set up parameter passing to a subcircuit using SUBPARAM

1. Make the subcircuit your active schematic page in the Capture editor.
2. From the Place menu, choose the Part command.
3. Select the part SUBPARAM from the PSpice library SPECIAL.OLB and place it on the subcircuit.
4. With the SUBPARAM part still selected, from the Edit menu, choose Properties.
   The Property Editor spreadsheet appears.
5. In the spreadsheet, define the names and default values for the properties that can be changed on an instance-by-instance basis.
6. In the top-level schematic, use the Property Editor spreadsheet to edit the properties of the hierarchical part or block that references the subcircuit (child) schematic so they match the properties you defined in Step 5.

Any part in the subcircuit (child) schematic can reference the properties in its PSPICETEMPLATE. The PSpice subcircuit mechanism supports parameterizing:

- constants specified on device statements
- model parameters
• expressions consisting of constants
• parameters
• functions

Creating the netlist

You can generate a simulation netlist in one of two ways:

• from Capture’s Project Manager by using the Create Netlist command under the Tools menu. (If this is the first time you’re creating a hierarchical netlist for this project, you can only use this method.)
  - or -

• directly from within Capture itself by using the Create Netlist command under the PSpice menu.

During the netlist process, Capture creates several files with different extensions: the .NET file contains the netlist; the .CIR file contains simulation commands; and the .ALS file contains alias information.

To create a flat netlist

1 In the Capture Project manager, select the design file (.DSN) you want to netlist.
2 From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3 Select the PSpice tab.
4 Under the Options frame, leave all the checkboxes blank.
5 In the Netlist File text box, type a name for the output file, or click the Browse button to assign a filename.
6 If desired, click the View Output checkbox to display the netlist after it has been generated.
7 Click OK.
To create a hierarchical netlist

1. In the Capture Project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. Under the Options frame, click Create Hierarchical Format Netlist.
5. Click Settings to customize the format of the hierarchical netlist (see Customizing the hierarchical netlist on page 294).
6. Click Create Subcircuit Format Netlist to specify how subcircuits will be netlisted (see Creating subcircuit netlists on page 297).
7. In the Use Template list box, select the netlisting template(s) you wish to apply (see Specifying alternate netlist templates on page 297).
8. In the Netlist File text box, type a name for the output file, or click the Browse button to assign a filename.
9. If desired, click the View Output checkbox to display the netlist after it has been generated.
10. Click OK.

For more information on netlist formats, refer to OrCAD Capture’s online help.

Customizing the hierarchical netlist

You can customize the hierarchical netlist by specifying various options using the Settings button in the Create Netlist dialog box. You can also customize the format of the subcircuit definition and reference text in the netlist. These settings, once defined, will apply to all subsequent PSpice netlists whether the netlist is invoked from the Tools menu in the Project Manager or directly from the schematic editor.

For more information on netlist formats, refer to OrCAD Capture’s online help.
Two groups of settings are saved: PSpice and LVS. Having two groups makes it easy to switch between netlisting for PSpice and netlisting for an LVS compatible format. You can specify which group of settings is active for the netlister by using the Products list box.

**Note** The settings you define are project specific. If you want to save the settings globally, click the Save as Default Project Settings button.

**To customize the hierarchical netlist**

1. In the PSpice tab of the Create Netlist dialog box, under the Options frame, click Create Hierarchical Format Netlist.

2. Click Settings, then enable or specify the following options, as desired:
   - Make .PARAM Commands Global: If this checkbox is enabled, any param parts in the design become global in scope. If it is disabled, the param parts are local to the subcircuit in which they occur.
   - Products: This list box specifies which group of settings is active for the netlister. Selecting a different group changes the Subcircuit Patterns frame to reflect the settings of the specified tool.
Global Net Prefix: This text box allows you to define the syntax of the global net of a subcircuit.

Reference frame
- Subcircuit Call: This list box allows you to select the syntax of the subcircuit call using a modified TEMPLATE syntax.
- ParamList Element Definition: This list box allows you to select the syntax of how parameters are passed from a reference to a part definition.

Definition frame
- Subcircuit Header: This list box allows you to select the syntax of the subcircuit header using a modified TEMPLATE syntax. If modified, you must make sure the definition header is consistent with the call.
- ParamList Element Definition: This list box allows you to select the syntax of how parameters are passed from a reference to a part definition.
- Param Usage Reference: This list box allows you to select the syntax used to enclose the parameters in references.
- Subcircuit Ends: This list box allows you to select the syntax used for the termination of a subcircuit.
- Save as Project Default Settings: This button saves the current settings in the CAPTURE.INI file, and thereby makes the current settings the default settings for any new Capture projects.

Click OK.

For more detailed information about the syntax for these commands, and examples of how to use them, see the OrCAD PSpice A/D Reference Guide.
Creating subcircuit netlists

You can specify how subcircuits in a hierarchical design are processed and defined in the simulation netlist.

To create a subcircuit format netlist

1. In the Capture Project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4. Under the Options frame, click Create Subcircuit Format Netlist, then click one of the following options, as desired:
   - Descend: This generates a definition of a hierarchical design that includes the top level circuit as well as its subcircuits. (This option is only available if Create Hierarchical Format Netlist is enabled.)
   - Do Not Descend: This generates a definition of a hierarchical design that includes only the top level circuit, without any of its subcircuits. (This option is only available if Create Hierarchical Format Netlist is enabled.)
   - Descend and Fully Expand: This generates a definition of a flat design. (This option is only available if Create Hierarchical Format Netlist is not enabled.)

Specifying alternate netlist templates

To specify an alternate netlist template

1. In the Capture Project manager, select the design file (.DSN) you want to netlist.
2. From the Tools menu, choose Create Netlist to display the Create Netlist dialog box.
3. Select the PSpice tab.
4 In the Use Template list box, select the name of the template you want to use.

By default, the netlister will use the PSPICETEMPLATE. Alternate templates in the Use Template list box will be processed in the order in which they appear. The ordering of the templates is therefore important to the netlister and determines what the output will be.

Use the control buttons located directly above the Use Template list box to configure the list of templates. You can:

- add a new template by clicking the New icon or by double-clicking in the dashed box at the beginning of the list.
- delete a template by selecting the name and then clicking the Delete icon.
- edit a template name by selecting the name and then clicking the Edit icon.
Starting a simulation

- change the order of the listing (move a template up or down in the listing) by selecting the name and clicking the Up or Down arrows.

Note  Templates are not specific to either a flat or hierarchical netlist. The same template may be used for both types.

Starting a simulation from Capture

After you have set up the analyses for the circuit, you can start a simulation from Capture in either of the following ways:

- From the PSpice menu select Run.
- Click the Simulate button on the PSpice toolbar.

Starting a simulation outside of Capture

To start PSpice A/D outside of Capture

1. From the Start menu, point to the OrCAD program group, then choose PSpice A/D.
2. From the File menu, choose Open Simulation.
3. Do one of the following:
   - Double-click on the simulation profile filename (*.SIM) in the list box.
   - Enter the simulation profile filename (*.SIM) in the File name text box and click Open.
4. From the Simulation menu, choose Edit Settings to modify any of the analysis setup parameters.
5. From the Simulation menu, choose Run (or click the Run toolbar button) to begin the simulation.
Setting up batch simulations

Multiple simulations can be run in batch mode when starting PSpice A/D directly with circuit file input. You can use batch mode, for example, to run a number of simulations overnight. There are two ways to do this, as described below.

Multiple simulation setups within one circuit file

Multiple circuit/simulation descriptions can be concatenated into a single circuit file and simulated all at once with PSpice A/D. Each circuit/simulation description in the file must begin with a title line and end with a .END statement.

The simulator reads all the circuits in the circuit file and then processes each one in sequence. The data file and simulation output file contain the outputs from each circuit in the same order as they appeared in the circuit file. The effect is the same as if you had run each circuit separately and then concatenated all of the outputs.

Running simulations with multiple circuit files

You can direct PSpice A/D to simulate multiple circuit files using either of the following methods.

Method 1

1. From the Start menu, point to the OrCAD program group, then choose PSpice A/D.
2. Select Open Simulation from the File menu from the PSpice A/D window.
3. Do one of the following:
   - Type each file name in the File Name text box separated by a space.
   - Use the combination keystrokes and mouse clicks in the list box as follows: [Ctrl]+click to select file names one at a time, and [Shift]+click to select groups of files.
Method 2

1. From the Start menu, point to the OrCAD program group, then choose PSpice A/D.

2. Update the command line in the following way:
   - Include a list of circuit file names separated by spaces.
   
   Circuit file names can be fully qualified or can contain the wild card characters (* and ?).

The PSpice A/D simulation window

The PSpice A/D Simulation Window is an MDI (Multiple Document Interface) application. This implies that you can open and display multiple files at the same time in this window. For instance, you can have a waveform file (.DAT), a circuit file (.CIR), and a simulation output file (.OUT) open and displayed in different child windows within this one window.

The PSpice A/D Simulation Window consists of three sections: the main window section where the open files are displayed, the output window section where output information such as informational, warning, and error messages from the simulator are shown, and the simulation status window section where detailed status information about the simulation are shown. These three sections are shown in Figure 56.

The windows in these sections may be resized, moved, and reordered as needed.

The simulation window also includes a menu bar and toolbars for controlling the simulation and the waveform display.

Title bar  The title bar of the simulation window (the area at the top of the window) identifies the name of the currently open simulation (either simulation profile or circuit file) and the name of the currently active document.
displayed in the main window area. For example, the simulation window shown in Figure 56 indicates that simulation profile Example-TRAN is currently open and the active document displayed is Example-Example-TRAN.DAT.

**Menus and Toolbars**  The menus accessed from the menu bar include commands to set up and control the simulator, customize the window display characteristics, and configure the way the waveforms are displayed. The toolbar buttons duplicate many of the more frequently used commands.

![Figure 56  PSpice A/D simulation window](image)

**Main window section**  The top central portion (by default) of the simulation window is the main window section where documents (such as waveforms, circuit description, output information etc.) are displayed within child windows. These windows are tabbed by default. The tabs at the bottom left show the names of the documents that each child window contains. Clicking on a tab brings that child window to the foreground. Figure 56 shows the tabbed document windows for
Example-Example-TRAN.DAT and Example-Example-TRAN.OUT.

You can configure the display of these windows to suit your preferences and to make the analysis of the circuit quick and readily understandable. These windows can also be resized, moved, and reordered to suit your needs.

**Output window section**  The lower left portion of the simulation window provides a listing of the output from the simulation. It shows informational, warning, and error messages from the simulation. You can resize and relocate this window to make it easier to read.

**Simulation status window section**  The lower right portion of the simulation window presents a set of tabbed windows that show detailed status about the simulation. There are three tabbed windows in this section: the Analysis window, the Watch Variable window, and the Devices window. The Analysis window provides a running log of values of simulation variables (parameters such as Temperature, Time Step, and Time). The Watch Variable window displays watch variables and their values. These are the variables setup to be monitored during simulation. The Devices window displays the devices that are being simulated.